# **Step by Step Implementation**

This will give you a visual demonstration for the implementation. Please skip this if you are familiar with Verilog synthesis and simulation platforms. Here we are using Quartus II (or Quartus Prime is possible) and ModelSim.

First go to the extracted folder and open “uart\_tx\_rx.qpf”.

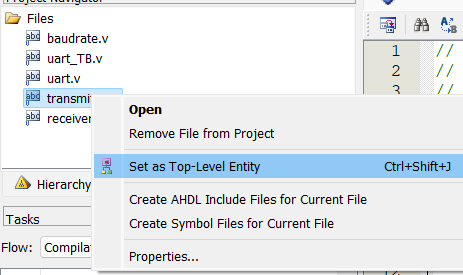


Then we can go to the codes by going into files.

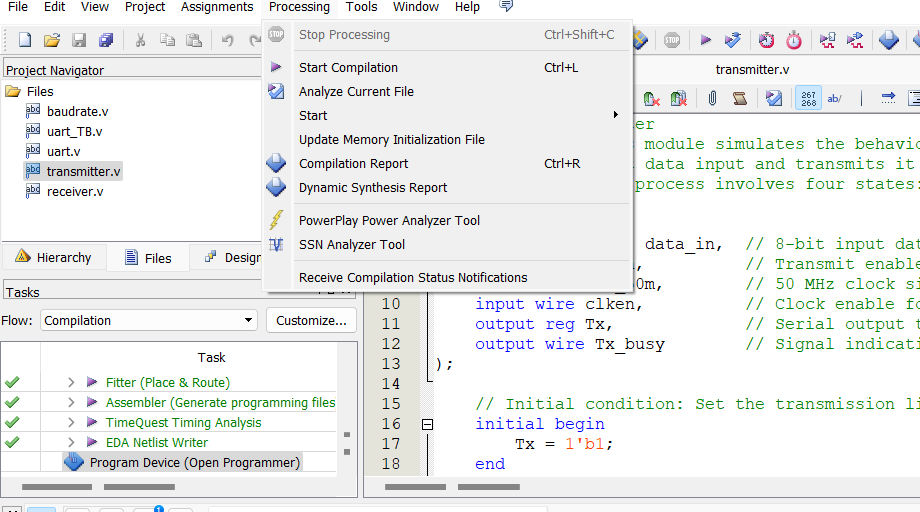
A screenshot of a computer

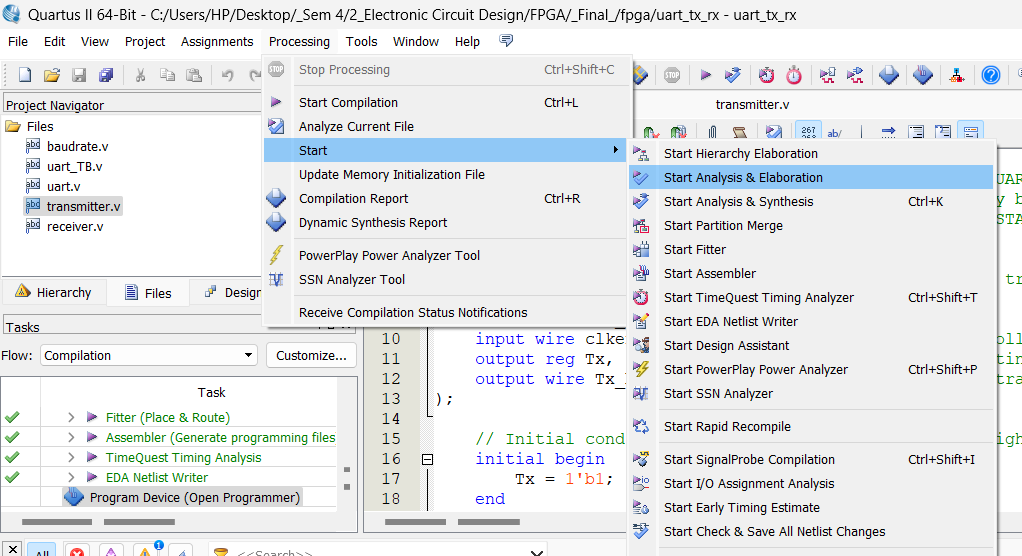
Description automatically generated

Here I will show you how to synthesis the transmitter. Similar manner you can try receiver, baudrate and uart files. Do not try to synthesis uart\_TB since it is the simulation. Please make sure you set top level entity the file you need to synthesis.

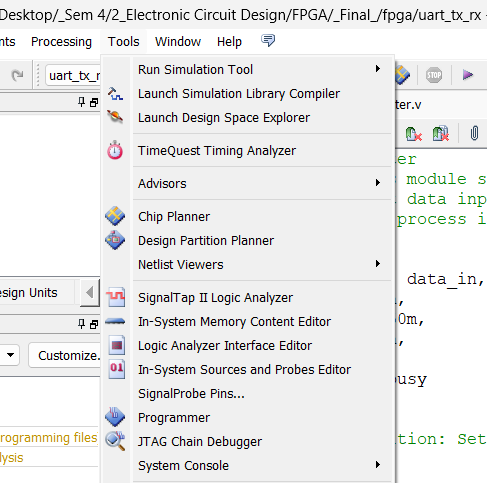


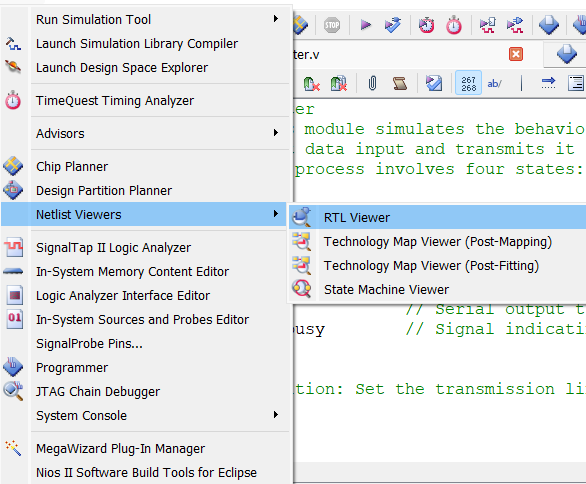
Then to synthesis circuit virtually, go to Start >> Start Analysis & Elaboration.

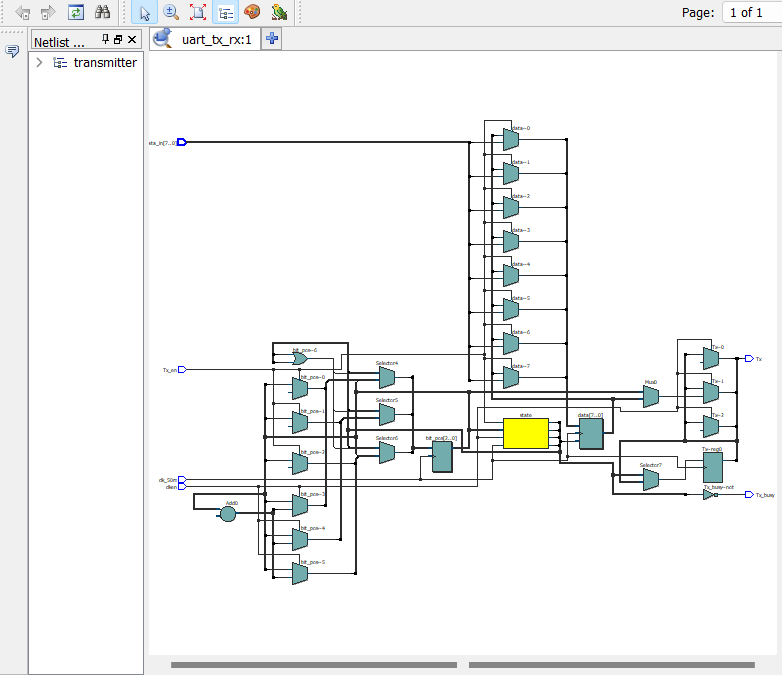




Go to Tools >> Netlist Viewers >> RTL Viewer to view the synthesized circuit for the transmitter.

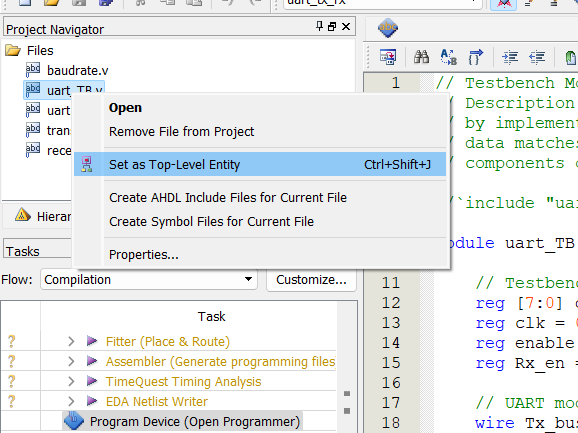


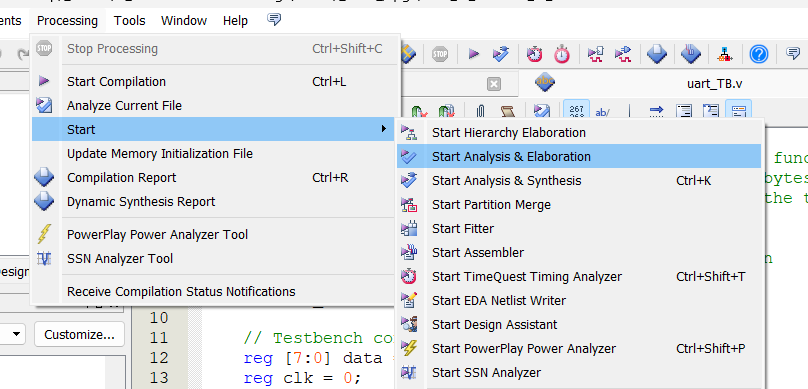




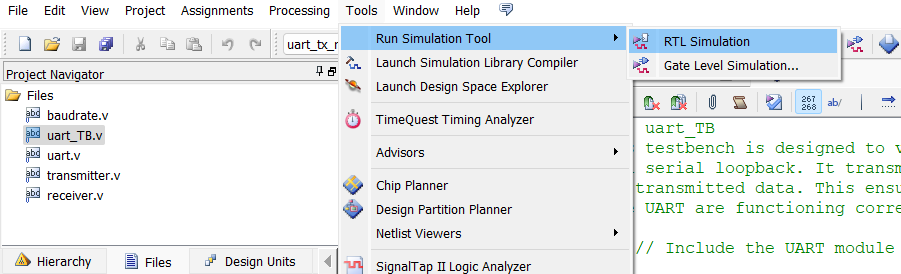
In similar way, you can try other synthesis files too.

Then let us see how to simulate the testbench. The given testbench is for the main uart circuit. But you can implement test benches for other circuits too. Just do and play with it. Please make sure you analyzed and elaborated all the circuits before this testbench simulation.

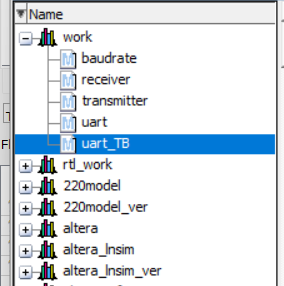
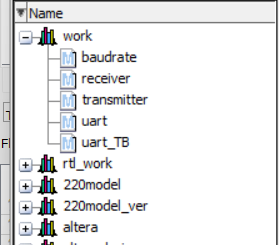




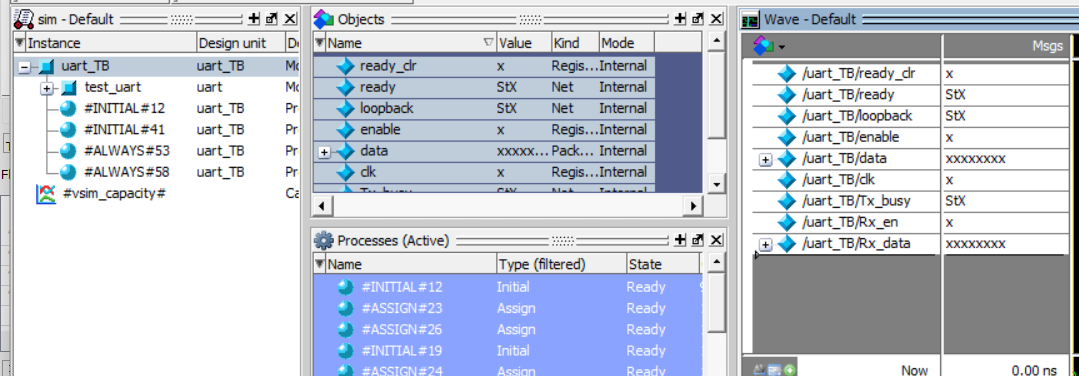
Now it is time for simulation.



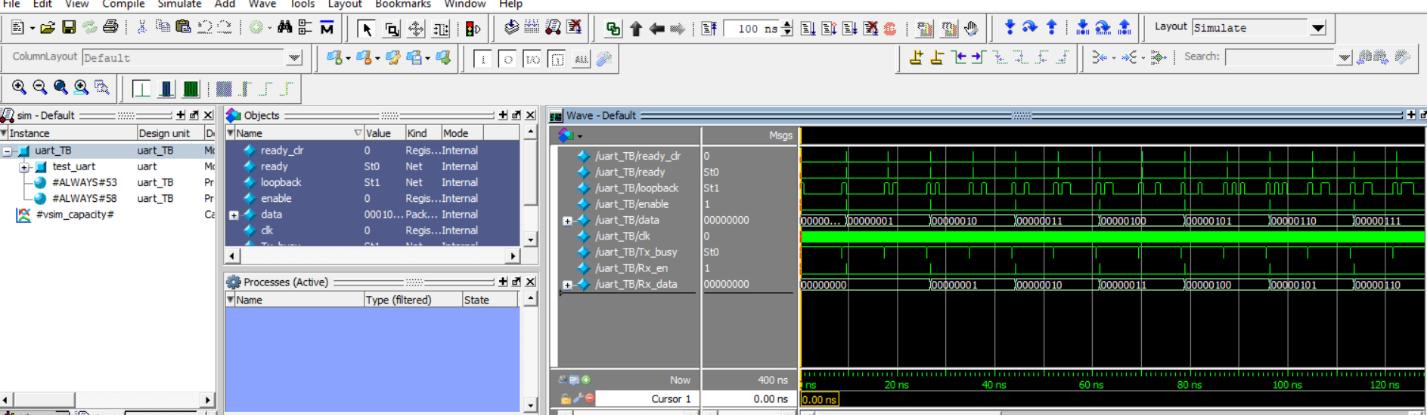
In ModelSim, expand work directory and double click on uart\_TB(testbench).



Then drag and drop all the entities in Objects bar to Wave bar. (Use CTRL + A to easily drag and drop)



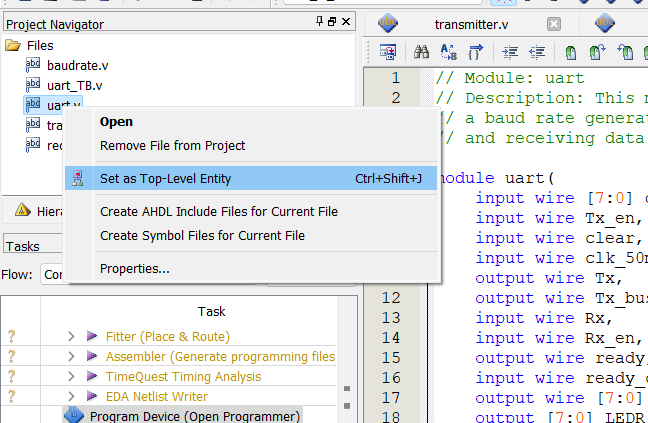
Set the simulation time as 100ns and run several times.

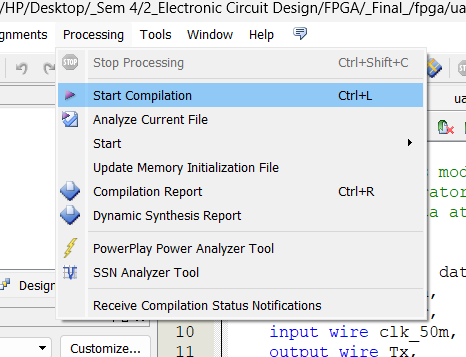


You can try more testbenches and simulate similar way.

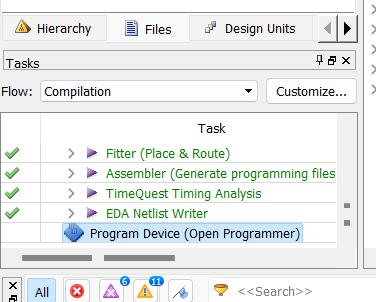
Now it is time to upload the code into FPGA and simulate. We have used EP4CE22F17 FPGA within the Cyclone IV E family. So, pin assignments correspond to that. If you are using another type of FPGA, then use the corresponding datasheet for pin assignments.

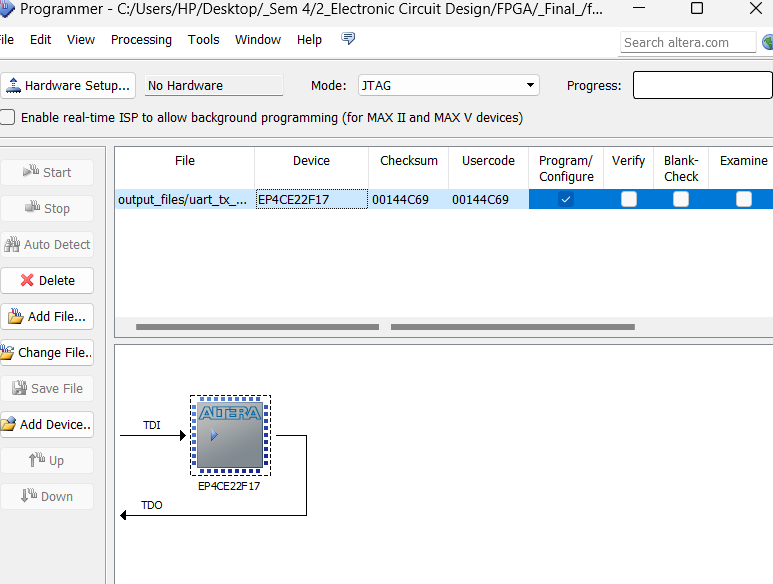
First set uart file as top level and compile.



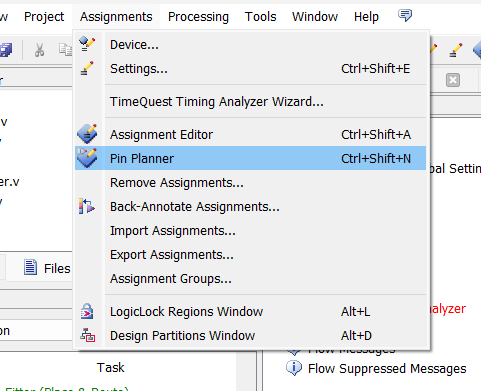


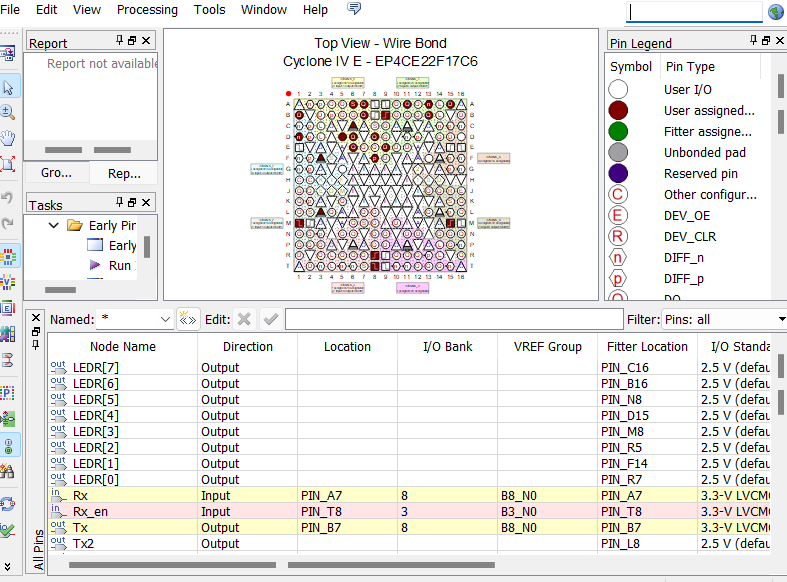
After the successful compilation, go to the Program Device and detect your FPGA. Finally upload the code into FPGA.





For pin planning use the steps below. You must have assigned pins before you are uploading the code into FPGA.





Use inbuilt LEDs in FPGA and Vcc and Ground from the same FPGA for your demonstration.